In re Patent Application of
MIRABEL ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**
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In the Claims:

Claims 1-14 (cancelled).

15. (new) A method of controlling a memory cell in an EEPROM, the memory cell comprising a floating gate transistor comprising a first conducting terminal and a control gate, the method comprising:

setting a state of the memory cell by simultaneously applying voltage pulses of opposite polarities respectively to the first conducting terminal and to the control gate;

each of the voltage pulses including a first portion having a slope greater than K*8 megavolts/second and a second portion having a slope between K*1 kilovolts/second and K*1 megavolts/second, with K=1 when the voltage pulse has a positive polarity and with K=-1 when the voltage pulse has a negative polarity.

16. (new) A method according to Claim 15, wherein the first conducting terminal defines a drain of the floating gate transistor.

17. (new) A method according to Claim 15, wherein each of the voltage pulses further includes a third portion having a substantially zero slope.

18. (new) A method according to Claim 17, wherein each of the voltage pulses further includes a fourth portion having a slope less than K*16 megavolts/second.

19. (new) A method according to Claim 15, wherein setting the state of the memory cell comprises a programming

step; and wherein the voltage pulses applied to the control gate are negative and the voltage pulses applied to the first conducting terminal are positive.

20. (new) A method according to Claim 15, wherein setting the state of the memory cell comprises an erasing step; and wherein the voltage pulses applied to the control gate are positive and the voltage pulses applied to the first conducting terminal are negative.

21. (new) A method according to Claim 15, wherein the simultaneously applied voltage pulses have equal amplitudes.

22. (new) A method according to Claim 15, wherein the EEPROM comprises a substrate with the floating gate transistor formed therein; and further comprising applying to the substrate voltage pulses equal to those being applied to the first conducting terminal.

23. (new) A method according to Claim 22, wherein the polarities of the applied voltage pulses are defined relative to a reference voltage; and wherein the substrate is grounded for providing the reference voltage.

24. (new) A method according to Claim 15, wherein the applied voltage pulses each have an amplitude that is less than 10 volts.

25. (new) A method according to Claim 15, wherein the applied voltage pulses have a potential difference within

a range of about 12 to 16 volts.

26. (new) A method according to Claim 15, wherein the memory cell further comprises a selection transistor comprising a first conducting terminal connected to the first conducting terminal of the floating gate transistor, and a gate; and further comprising applying voltage pulses of less than 12 volts to the gate of the selection transistor when setting the state of the memory cell.

27. (new) A method according to Claim 26, wherein the first conducting terminal of the selection transistor defines a source thereof.

28. (new) A method according to Claim 26, wherein the voltage pulses applied to the first conducting terminal of the selection transistor and to the first conducting terminal of the floating gate transistor have a same polarity.

29. (new) A method of controlling a memory cell comprising a storage transistor, the storage transistor comprising a first conducting terminal and a control gate, the method comprising:

setting a state of the memory cell by simultaneously applying voltage pulses of opposite polarities respectively to the first conducting terminal and to the control gate;

each of the voltage pulses including a first portion having a slope greater than K*8 megavolts/second, a second portion having a slope between K*1 kilovolts/second and K*1 megavolts/second, a third portion having a substantially zero slope, and a fourth portion having a slope less than K*16

megavolts/second, with K=1 when the voltage pulse has a positive polarity and with K=-1 when the voltage pulse has a negative polarity.

30. (new) A method according to Claim 29, wherein the memory cell is within an EEPROM; and wherein the storage transistor comprises a floating gate transistor and the first conducting terminal forms a drain thereof.

31. (new) A method according to Claim 29, wherein setting the state of the memory cell comprises a programming step; and wherein the voltage pulses applied to the control gate are negative and the voltage pulses applied to the first conducting terminal are positive.

32. (new) A method according to Claim 29, wherein setting the state of the memory cell comprises an erasing step; and wherein the voltage pulses applied to the control gate are positive and the voltage pulses applied to the first conducting terminal are negative.

33. (new) A method according to Claim 29, wherein the simultaneously applied voltage pulses have equal amplitudes.

34. (new) A method according to Claim 29, wherein the applied voltage pulses have an amplitude that is less than 10 volts; and wherein the applied voltage pulses have a potential difference within a range of about 12 to 16 volts.

35. (new) A method according to Claim 29, wherein

the memory cell further comprises a selection transistor comprising a first conducting terminal connected to the first conducting terminal of the floating gate transistor, and a gate; and further comprising applying voltage pulses of less than 12 volts to the gate of the selection transistor when setting the state of the memory cell.

36. (new) A method according to Claim 35, wherein the voltage pulses applied to the first conducting terminal of the selection transistor and to the first conducting terminal of the floating gate transistor have a same polarity.

37. (new) An electronic device comprising:

an EEPROM comprising a plurality of memory cells, each memory cell comprising a floating gate transistor comprising a first conducting terminal and a control gate; and

at least one power supply for simultaneously applying voltage pulses of opposite polarities respectively to the first conducting terminal and to the control gate of a selected memory cell when setting a state thereof;

each of the voltage pulses including a first portion having a slope greater than K*8 megavolts/second and a second portion having a slope between K*1 kilovolts/second and K*1 megavolts/second, with K=1 when the voltage pulse has a positive polarity and with K=-1 when the voltage pulse has a negative polarity.

38. (new) An electronic device according to Claim 37, wherein said EEPROM comprises a P-type substrate with said plurality of memory cells formed therein, said P-type substrate comprising a plurality of N-type isolation wells for

isolating a plurality of P-type wells, each P-type well including a respective memory cell therein.

39. (new) An electronic device according to Claim 37, wherein the first conducting terminal defines a drain of said floating gate transistor.

40. (new) An electronic device according to Claim 37, wherein each of the voltage pulses further includes a third portion having a substantially zero slope, and a fourth portion having a slope less than K*16 megavolts/second.

41. (new) An electronic device according to Claim 37, wherein setting the state of the selected memory cell comprises a programming step; and wherein the voltage pulses applied to the control gate are negative and the voltage pulses applied to the first conducting terminal are positive.

42. (new) An electronic device according to Claim 37, wherein setting the state of the selected memory cell comprises an erasing step; and wherein the voltage pulses applied to the control gate are positive and the voltage pulses applied to the first conducting terminal are negative.

43. (new) An electronic device according to Claim 37, wherein the simultaneously applied voltage pulses have equal amplitudes.

44. (new) An electronic device according to Claim 38, wherein said at least one power supply cell also applies to said P-type substrate voltage pulses equal to those being

applied to the first conducting terminal.

45. (new) An electronic device according to Claim 44, wherein the polarities of the applied voltage pulses are defined relative to a reference voltage; and wherein said substrate is grounded for providing the reference voltage.

46. (new) An electronic device according to Claim 37, wherein the applied voltage pulses each have an amplitude that is less than 10 volts.

47. (new) An electronic device according to Claim 37, wherein the applied voltage pulses have a potential difference within a range of about 12 to 16 volts.

48. (new) An electronic device according to Claim 37, wherein said EEPROM further comprises a plurality of selection transistors, each selection transistor comprising a first conducting terminal connected to the first conducting terminal of a respective floating gate transistor, and a gate; and wherein said at least one power supply cell also applies voltage pulses of less than 12 volts to the gate of said selection transistor when setting the state of the selected memory cell.

49. (new) An electronic device according to Claim 48, wherein the voltage pulses applied to the first conducting terminal of said selection transistor and to the first conducting terminal of said floating gate transistor have a same polarity.